REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 6-10, 15-18, and 26-68 are presently active, with Claims 6-10 and 15-18 withdrawn as directed to a non-elected invention. Claims 1-3, 5, 11-14, and 19-25 have been cancelled without prejudice; and Claims 26-68 have been added by the present amendment. The additions to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, the title of the invention was objected to as being non-descriptive of the claimed invention. In addition, Claims 1-3 and 5 were rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 4,495,693 to Iwahashi et al. (hereinafter "the '693 patent"), in view of published U.S. Patent Application No. 2001/0002711 A1 to Gonzalez (hereinafter "the '711 application").[3] Further, Claims 11, 14, 19, and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '693 patent and '711 application, further in view of U.S. Patent No. 4,769,340 to Chang et al. (hereinafter "the '340 patent") and U.S. Patent No. 4,866,003 to Yokoi et al. (hereinafter "the '003 patent"). Finally, Claims 12, 13, and 21-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '693 patent, the '711 application, the '340 patent, and the '003 patent, further in view of U.S. Patent No. 4,467,452 to Saito et al. (hereinafter "the '452 patent") and U.S. Patent No. 5,731,130 to Tseng (hereinafter "the '130 patent").

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[3]Applicants note that a rejection under 35 U.S.C. § 102(b) over a combination of references is improper. Accordingly, Applicants will assume that Claims 1-3 and 5 are rejected under 35 U.S.C. § 103(a) only.

In response to the objection to the title, the title has been amended to be more descriptive of the claimed invention. Accordingly, the objection to the title is believed to have been overcome.

Applicants respectfully submit that the rejections of Claims 1-3, 5, 11-14, and 19-25 under 35 U.S.C. § 103 are rendered moot by the cancellation of those claims herein.

The present amendment also sets forth new Claims 26-68 for examination on the merits. Claim 26 is directed to a non-volatile semiconductor memory device, comprising: (1) a semiconductor substrate having a peripheral circuit region and a memory cell region; (2) a first element region provided in the peripheral circuit region; (3) a second element region provided in the memory cell region; (4) a first element isolation region provided in the semiconductor substrate, the first element isolation region isolating the first element region; (5) a second element isolation region provided in the semiconductor substrate, the second element isolation region isolating the second element region; (6) a first transistor having source and drain diffusion layers each provided in the first element region; (7) a second transistor having source and drain diffusion layers each provided in the second element region; and (8) an insulating film covering the first and second transistors, the insulating film being harder for an oxidizing agent to pass therethrough, compared with a silicon oxide film, the insulating film being oxidized. New Claim 26 is supported by the originally filed specification and does not add new matter.[4]

Further, Applicants submit that the new Claim 26 patentably defines over the references applied by the Office Action in rejecting canceled Claims 1-3, 5, 11-14, and 19-25.

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[4]See, e.g., Figures 3a and 3b and the written description related thereto.

The '693 patent is directed to a semiconductor memory device having an MOS transistor and a floating-gate-type MOS transistor. Referring to Figure 11L, the Office Action indicates that the '693 patent discloses an insulating film 158 covering a second transistor. However, the '693 patent fails to disclose that the insulating film 158 is *harder for an oxidizing agent to pass therethrough as compared to a silicon oxide film*, as recited in new Claim 26.

The '711 application is directed to an improved storage node junction in a DRAM memory cell. The '711 application discloses a first insulating film 30 that reduces the area of the storage node junction 43. However, Applicants submit that the '711 insulating film 30 does not cover first and second transistors.

The '340 patent is asserted by the Office Action merely to disclose "erasable and programmable memory cell transistors." However, Applicants submit that the '340 patent fails to disclose the insulating film recited in new Claim 26.

The '003 patent is directed to a semiconductor device having a passivation film with an improved hot-carrier resistivity. The '003 patent discloses a silicon nitride film 12 with a hydrogen-bonded-silicon concentration of 5×10^{21} atoms/cm^3 or lower. The silicon nitride film 12 is formed by a plasma-assisted CVD process, and is *not oxidized.* Thus, the '003 patent fails to disclose an insulating film covering the first and second transistors, wherein the insulating film is oxidized, as recited in Claim 26.

Accordingly, Applicants respectfully submit that the '693 patent, '711 application, '340 patent, and '003 patent, taken either singly or in proper combination, fail to disclose the insulating film recited in new Claim 26. Accordingly, Applicants respectfully submit that new Claim 26 (and dependent Claims 27-44) patentably define over the '693 patent, the '711 application, the '340 patent, and the '003 patent.

New Claim 45 recites limitations analogous to the limitations recited in new Claim 26. Accordingly, new Claim 45 is also supported by the originally filed specification and does not add new matter. Moreover, for the reasons stated above for the patentability of new Claim 26, Applicants respectfully submit that Claim 45 (and dependent Claims 46-68) patentably define over the '693 patent, the '711 application, the '340 patent, and the '003 patent.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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Serial No: 09/556,777
Amendment Filed: 3-4-3

IN THE TITLE

Please replace the Title of the Invention with the following Title:

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE [AND METHOD FOR MANUFACTURING THE SAME] COVERED WITH INSULATING FILM WHICH IS HARD FOR AN OXIDIZING AGENT TO PASS THERETHROUGH

IN THE SPECIFICATION

Please amend the paragraph beginning on page 5, line 17, as follows:

A nonvolatile semiconductor memory device according to an aspect of the invention comprises: a semiconductor substrate having a peripheral circuit region and a memory cell region; a first element region provided in the peripheral circuit region; a second element region provided in the memory cell region; a first element isolation region provided in the semiconductor substrate, the first element isolation region isolating the first element region; a second element isolation region provided in the semiconductor substrate, the second element isolation region isolating the second element region; a first transistor having source and drain diffusion layers each provided in the first element region; a second transistor having source and drain diffusion layers each provided in the second element region; and an insulating film covering the first and second transistors, the insulating film being harder for an oxidizing

agent to pass therethrough, compared with a silicon oxide film, and the insulating film being oxidized [A nonvolatile semiconductor memory device according to an aspect of the present invention comprises: a semiconductor substrate; and element isolation region formed in the semiconductor substrate, the element isolation region isolating a plurality of element regions in the semiconductor substrate; a first transistor formed in a peripheral circuit portion of the semiconductor substrate, the first transistor including source and drain diffusion layers formed in one of the plurality of element regions and a gate electrode having a first gate length, a second transistor formed in a memory cell portion of the semiconductor substrate, the second transistor including source and drain diffusion layers formed in another of the plurality of element regions and a gate electrode having a second gate length shorter than the first gate length; a contact connected to the one of the source and drain diffusion layers; and a first insulating film different from a silicon oxide covering the second transistor and not covering the first transistor, the first insulating film being an etching stopper for the contact to the element isolation region and having a property which makes it difficult for an oxidizing agent to pass therethrough compared with the silicon oxide].

IN THE CLAIMS

1-3. (Canceled)

5. (Canceled)

11-14. (Canceled)

19-25. (Canceled)

26-68. (New)

IN THE ABSTRACT

Please amend the Abstract on page 38 as follows:

[A first transistor formed in a peripheral circuit portion of a semiconductor substrate. The first transistor includes source and drain diffusion layers formed in one element region. A second transistor formed in a memory cell portion of the semiconductor substrate. The second transistor includes source and drain diffusion layers in another element region. A contact connected to the one of the source and drain diffusion layers. A first insulating film different from a silicon oxide covers the second transistor. The first insulating film is an etching stopper for the contact to the element isolation region and has a property which makes it difficult for an oxidizing agent to pass therethrough compared with the silicon oxide] A nonvolatile semiconductor memory device includes a first element region provided in a peripheral circuit region of a semiconductor substrate; a second element region provided in a memory cell region of the substrate; a first element isolation region provided in the substrate; a second element isolation region provided in the substrate; a first transistor having source and drain diffusion layers each provided in the first element region; a second transistor having source and drain diffusion layers each provided in the second element region; and an insulating film covering the first and second transistors. The insulating film is harder for an oxidizing agent to pass therethrough, compared with a silicon oxide film, and the insulating film is oxidized.

ABSTRACT

A nonvolatile semiconductor memory device includes a first element region provided in a peripheral circuit region of a semiconductor substrate; a second element region provided in a memory cell region of the substrate; a first element isolation region provided in the substrate; a second element isolation region provided in the substrate; a first transistor having source and drain diffusion layers each provided in the first element region; a second transistor having source and drain diffusion layers each provided in the second element region; and an insulating film covering the first and second transistors. The insulating film is harder for an oxidizing agent to pass therethrough, compared with a silicon oxide film, and the insulating film is oxidized.